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For

# OPTIMAL SIMULTANEOUS DESIGN AND FLOORPLANNING OF INTEGRATED CIRCUIT


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# OPTIMAL SIMULTANEOUS DESIGN AND FLOORPLANNING OF INTEGRATED CIRCUIT

## BACKGROUND

**[0001]** The invention relates to computer aided design of integrated circuits, particularly the simultaneous determination for circuit parameters which include boundaries for floorplan layout.

## PRIOR ART

**[0002]** One computer aided design (CAD) technique for designing integrated circuits, particularly analog circuits, relies upon geometric programming. In general, posynomial expressions of circuit parameters for a plurality of performance specifications are first developed. These expressions are constrained, typically by optimization values for a selected one or more of the performance specifications. The expressions are then solved using geometric programming. This solution provides a globally optimal design. Among the specified performance criteria are layout area, gate overdrive, minimum power, unity gain bandwith, etc. . . Dimensional constraints such as symmetry and matching, limits on device size and total area are used. For a discussion of this technology, see *System And Method For Designing Circuits*, Serial No. 09/123,129, filed July 27, 1998.

**[0003]** The present invention is an extension of this technology which provides simultaneously with the above computation, specific boundaries in the floorplan of the circuit elements in the integrated circuit.

SUMMARY OF THE INVENTION

**[0004]** The present invention is a method for designing an integrated circuit where design parameters for performance specifications are represented by posynomial expressions with constraints and then solved with geometric programming. The present invention provides an improvement where simultaneous determination of the boundaries for circuit elements in a floorplan result. The floorplan is represented as posynomial expressions with constraint on the size of each of the circuit elements. These posynomial expressions are solved using geometric programming thereby providing the boundaries within the floorplan simultaneously with determining the circuit parameters for the performance specifications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] **Figure 1** is a flow diagram showing the steps of the present invention.

[0006] **Figure 2** is a flow diagram showing the method for obtaining the posynomial expressions for each of the circuit element using a slicing technique.

[0007] **Figure 3** is a circuit diagram of an integrated circuit.

[0008] **Figure 4** is a floorplan layout for the circuit of Figure 3.

[0009] **Figure 5** is a slicing diagram for the floorplan of Figure 4.

[0010] **Figure 6** is a floorplan layout for another integrated circuit.

[0011] **Figure 7** is a slicing diagram for the floorplan of Figure 6.

DETAILED DESCRIPTION

**[0012]** A method is described for providing the boundaries forming a floorplan for a circuit. In the following description, numerous specific details are set forth, such as specific circuits to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known prior art technique such as solving posynomial expressions using geometric program is not set forth in detail in order not to unnecessarily obscure the present invention.

**[0013]** In the following description, the word "posynomial" expression or equation is used. This term is used to include a monomial expression or equation.

**[0014]** In the prior art, it is known that the design of many different analog circuit cells such as operational amplifiers (op-amps), spiral inductors, and LC oscillators, as well as more complicated analog and mixed circuits, such as phase-lock loops, analog-to-digital and digital-to-analog converters and switched-capacitor filters can be cast as geometric programs. These designs presupposes the active devices are operating in their saturation regions. In this patent, this prior art technology is built upon in that the layout floorplanning constraints for a circuit are set forth in posynomial and hence, can be mixed with design constraints. This allows for the simultaneous design and floorplanning of analog circuits using geometric programming. Consequently, the design and floorplanning can be performed optimally in a single step.

**[0015]** In co-pending application 09/123,129; filed July 27, 1998; entitled *System and Method for Designing Integrated Circuits*, now U.S. Patent _____, the design techniques for designing for instance, an op-amp is described. In summary, this prior

art computer aided design (CAD) system provides for the design and in optimizing of integrating circuits. It results in the automated synthesis of globally optimal circuit designs for a give circuit topology resulting directly from a user defined specification. Generally, the CAD system includes a library of integrated circuit topologies. The performance specifications for the integrated circuit topologies are described as posynomial functions of the design parameters. The performance specifications are combined with user defined design objectives and constraints to form a geometric program. One embodiment reformulates geometric programs as convex optimization problems, i.e. the problem of minimizing a convex function subject to convex inequalities constraints and linear equality constraints. This facilitates globally and efficiently solving geometric programs. New variables $y_i = \log x_i$ are defined, the logarithm of a polynomial $f$ is taken to get

$$h(y)=\log(f(e^{y1},\ldots,e^{yn}))=\log\left(\sum_{k}^{t} e^{a_k^T y+b_k}\right)$$

**[0016]** where $a_k^T=[\alpha_{1k}\ldots\alpha_{nk}]$ and $b_k=\log c_k$. It can be shown that $h$ is a convex function of the new variable $y$: for all $y,z \in \mathbf{R}^n$ and $0\leq\lambda\leq 1$ which yields

$$h(\lambda y+(1-\lambda)z)\leq\lambda h(y)+(1-\lambda)h(z).$$

**[0017]** The geometric program is then expressed as convex program as follows:

$$\begin{array}{ll} \text{minimize} & \log f_0(e^{y1},\ldots,e^{yn}) \\ \text{subject to} & \log f_i(e^{y1},\ldots,e^{yn})\leq 0,\ i=1,\ldots,m \\ & \log g_i(e^{y1},\ldots,e^{yn})=0,\ i=1,\ldots,p. \end{array}$$

**[0018]** This is the so-called exponential form of the geometric program. The convexity of the exponential form geometric program has several important implications including that efficient interior-point methods can be used to solve such geometric programs, and there is a

complete and useful duality, or sensitivity theory for them. The efficient procedures for solving geometric programs typically provide the globally optimal results in a matter of seconds in a digital computer. The present invention therefore yields automated synthesis of globally optimal circuit designs for a given circuit topology library, directly from specifications.

**[0019]** With the present invention, the first step includes representing a circuit such as an op-amp as posynomial constraints as is described in the above referenced patent. Step 10 shows this in Figure 1 under the step "represent circuit design parameters by posynomial constraints."

**[0020]** Unlike the prior art, however, the present invention now represents the floorplan of the circuit such as an op-amp, as polynomial constraints of circuit element size. In effect, the boundaries of the circuit elements forming the circuit such as the transistors in an op-amp, are represented as posynomial expressions with constraints, as will be described.

**[0021]** Next, the expressions both for the floorplan and the performance specifications of the circuit represented by design parameters are solved with a geometric program yielding both the circuit parameters and the boundaries of the circuit elements in the floorplan. This is shown in Figure 1 as step 12. This can be done generally using a modern workstation in a matter of minutes. Such computation without a modern digital computer could take a lifetime to compete manually.

**[0022]** The results of step 12 are represented in a format which preferably can be readily used by a designer in the layout of the circuit for fabrication as an integrated circuit as shown by step 13. For instance, a computer readable format is provided on a specified grid identifying the circuit elements and their parameters such as the length and width of channels

of MOS transistors. In other instances, it may be more desirable to provide a hard copy with the fabrication information. In any event, the solution resulting from the geometric program enables the fabrication of an optimal circuit. In one embodiment, the circuit fabrication data is sent over the Internet to a designer that incorporates the design into an overall chip design. Then the chip incorporating the circuit designed in accordance with the present invention can be fabricated using known processes.

**[0023]** Consider first the op-amp of Figure 3. It is fabricated with n-channel, MOS transistors and a passive capacitor 34. The input devices $M_1$ and $M_2$ (transistors 30 and 31) are connected in series with their respective loads $M_3$ and $M_4$ (transistors 32 and 33). The two resultant legs are coupled to $M_5$ (transistor 37). A biasing potential is developed from the constant current source 35 which is coupled to the gate of $M_5$ through $M_6$ (transistor 36). The output capacitor $C_C$ is coupled to the common node between $M_2$ and $M_4$.

**[0024]** A suggested floorplan for this op-amp is shown in Figure 4. The active loads $M_3$ and $M_4$ of the op-amp are laid out in the upper left hand corner of the floorplan. The compensation capacitor $C_C$ is laid out on the right side of the floorplan. The input transistors $M_1$ and $M_2$ are shown laid out directly below $M_3$ and $M_4$. Finally, $M_5$ and $M_6$ are laid out along side each other in the lower left hand corner of the floorplan. Although the relative location of the different cells (e.g., $M_3$, $M_4$) are fixed in Figure 4, the exact location of the boundary between the different cells is not fixed. That is, the location of lines 40, 41, 42, and 43 is not fixed within the overall circuit layout.

**[0025]** Given the generic floorplan of the op-amp as shown in Figure 4, the circuit topology, and required objective parameters and specifications, the goal is to design the circuit (e.g., size the transistors) so that all specifications are met. These objectives and specifications

include electrical specification such as gain and bandwidth for op-amps, as well as specifications such as the aspect area of the layout. Minimizing the layout area results in a design with optimal cell packing.

**[0026]** In one embodiment, the floorplan is represented as posynomial constraints of circuit element size using a slicing tree. Referring to Figure 4, assume that for a first slice, a vertical slice is taken along line 40. The cell on the right (sibling node) is the capacitor $C_C$ and the cell on the left (other sibling node) contains the cells $M_3$, $M_4$; $M_1$, $M_2$; $M_5$; and $M_6$. Referring to Figure 5, this initial slice is shown beginning at node 0 by the lines 51 and 52. The "V" on these lines indicate a vertical slice. Line 51 is shown ending in the capacitor, whereas line 52 lead to the point for the next slice.

**[0027]** Now, a horizontal slice is made beginning at node 1 along line 41. As shown by line 53, this results in the sibling node, cell $M_3$, $M_4$. Line 54 leads to node 2 where the next slice occurs.

**[0028]** From node 2, an additional horizontal slice is made along line 42 as shown by lines 55 and 56 of Figure 5. Line 55 ends in the sibling node comprising the transistors $M_1$, $M_2$. Line 56 includes the two nodes, $M_5$ and $M_6$. Now, an additional vertical slice is made along line 43 as shown by lines 57 and 58 resulting in the sibling nodes, cells $M_5$ and $M_6$.

**[0029]** Suppose that $(x_i, y_i)$ are the horizontal dimension (width) and vertical dimension (height) respectively of the $i^{th}$ cell corresponding to the $i^{th}$ node of the slicing tree shown in Figure 5. Given the slicing tree, one can write the inequality constraints relating to the $(x_i, y_i)$. For example, at node 0

$$\begin{aligned} &\chi_1 + \chi_{cap}(C_c) \le \chi_0, \\ &y_1 \le y_0, \\ &y_{cap}(C_c) \le y_0, \end{aligned} \qquad (1)$$

**[0030]** where $\chi_{cap}(C_c)$ and $y_{cap}(C_c)$ are the width and the height of the capacitor $C_c$ respectively. Or at node 1:

$$\chi_{mir}(M_3, M_4) \leq \chi_1,$$

$$\chi_2 \leq \chi_1, \qquad (2)$$

$$y_{mir}(M_3, M_4) + y_2 \leq y_1,$$

**[0031]** This is summarized in Figure 2 beginning with block 20. For vertical slices as shown by block 22, the sum of the widths of the sibling nodes are equal to or less than the parent node, while the heights of the sibling nodes are each equal to or less than the parent node. In contrast, for the horizontal slice of block 21, the sum of the heights of the sibling nodes is equal to or less than the parent node, while the widths of the sibling nodes are each equal to or less than the parent node.

**[0032]** As indicated by the lines 23 and 24, slicing continues until the entire circuit is sliced into individual cells for which the boundaries are to be determined. When this is done as shown by block 25, the circuit elements such as the MOS transistors and the capacitor for the op-amp, are represented as a function of boundaries and other element parameters as will be described.

**[0033]** As can be seen, constraints such as shown by equations (1) and (2) are posynomial constraints in cell sizes of the variables ($x_i$ , $y_i$). There are also posynomial expressions in circuit variables (e.g., W, L of transistors, size of $C_c$, etc...) because the functions $\chi_1 + \chi_{cap}(C_c)$, $y_{cap}(C_c)$, $\chi_{mir}(M_3, M_4)$, and $y_{mir}(M_3, M_4)$ are all posynomial in the circuit variables as will be discussed later.

**[0034]** A constraint on the total area of the circuit to be less than $A_{spec}$, is simply given by:

**[0035]**
$$\chi_0 y_0 \leq A_{spect}, \qquad (3)$$

[0036] which is a monomial inequality in the variables ($\chi_0\ y_0$). Optimal packing of the cells is achieved by minimizing $\chi_0\ y_0$ which is a posynomial function of the variables.

[0037] A constraint on the aspect ratio of the circuit to be less than $\kappa_{spec}$ is given by:

[0038] $$\chi_0 / y_0 \leq \kappa_{1spec},\ y_0 / \chi_0 \leq \kappa_{2spect} \qquad (4)$$

[0039] The smallest aspect ratio can be found by minimizing max ($\chi_0\ y_0,\ y_0\ \chi_0$), which can then be converted into a geometric program (by introducing a slack variable).

[0040] Hence, by mixing the layout constraints which are posynomials, such as expressions (1), (2), (3), and (4) with the circuit constraints (as given in the above referenced patent), it is possible to optimally design the circuit and floorplan in one step.

[0041] Figures 6 and 7 illustrate another example of a circuit floorplan and slicing tree. In Figure 6, the circuit consists of transistors $M_1$, $M_2$, $M_3$, $M_4$, and $M_5$ with the illustrated topology.

[0042] Beginning with node 0, a horizontal slice along line 60 is made as shown by lines 71 and 72 of Figure 7. Line 72 ends in the cell $M_5$. Line 71 ends in the sibling nodes comprising $M_1$, $M_2$, $M_3$, and $M_4$. Next, at node 1, a horizontal slice along line 61 is made resulting in two sibling nodes: one at line 74 comprising transistors $M_3$ and $M_4$, and the other at line 73 comprising transistors $M_1$ and $M_2$. Now, a vertical slice is made along line 62 from node 2 resulting in cells $M_1$ and $M_2$ shown at the ends of lines 75 and 76 in Figure 7. Lastly, a horizontal slice is made along line 63 from node 3 resulting in the cells $M_3$ and $M_4$ shown at the ends of lines 77 and 78 of Figure 7.

[0043] Again, with each of the slices, the algorithm of Figure 2 is used. Specifically, for the vertical slices the sum of the widths of the sibling nodes is equal to or less than the parent node and the heights of the sibling nodes is equal to or less than the parent node. For the

horizontal slices, the sum of the heights of the sibling nodes is equal to or less than the parent node and the widths of the sibling nodes are each equal to or less than the parent node. From this, the posynomial expressions for each of the cell sizes can be written.

**[0044]** As mentioned earlier, the constraints represented by equations (1) and (2) above are posynomial constraints in the cell sizes in variables $\chi_i$, $y_i$. For each of the cells, posynomial expressions are used to represent the cell size in terms of the circuit element variables. For instance, in the case of a transistor, the width and length of the transistor.

**[0045]** Consider a MOS transistor *M*. A first approximation for the width and heights of the MOS is given by:

**[0046]**
$$\chi_{\text{nmos}}(M) = m_\chi L, \qquad y_{\text{mos}}(M) = m_y W,$$

**[0047]** which are monomial expressions in the circuit variables *L, W,* $m_\chi$, and $m_y$. Here *L* and *W* typically are the critical dimension in a fabrication process and *m* the number of counts for this dimension. These expressions only consider the active part of the MOS, and, for example, neglect the area of the contacts.

**[0048]** A better expression for the width and heights of *M* (NMOS in this case) is given by the posynomial equations:

$$x_{\text{mos}}(M) = \left(\frac{drainW}{2} + \frac{sourceW}{2} + L\right)m_x + 2\text{subSpX} + 2\text{subW} + \text{metalW}$$

$$y_{\text{mos}}(M) = m_x W + \frac{m_y}{2}\text{displ}_1 + \frac{m_y - 1}{2}\text{displ}_2 + 2\text{subSpY} + 2\text{subW}$$

**[0049]** where

drainW is the width of the drain

sourceW is the width of the source

metalW is the width of the metal lines around the transistor

subW is the width of the substrate contacts

subSpX is the horizontal distance form the transistor to the substrate contacts

subSpY is the vertical distance from the transistor to the substrate contacts

$displ_1$ is the distance from a line of fingers to the next, when a source connection is in between

$displ_2$ is the distance from a line of fingers to the next, when no source connection is in between

For other circuit elements such as differential pairs and current mirrors the equation are similar except that $m_x$ is multiplied by 2.

**[0050]** For example, the expression for a spiral inductor is described in "Optimization of Inductor Circuits Via Geometric Programming" Design Automation Conference, 1999 proceedings, 36, pps. 994-998 by M. Del Mar Hershenson, et al.

**[0051]** Thus, a method has been described for determining the boundaries in the floorplan of a circuit while simultaneously determining other design parameters using geometric programming.